

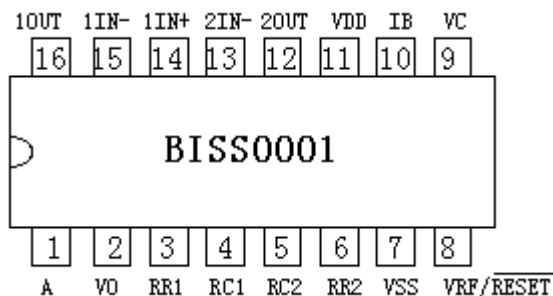
BISS0001

Micro Power PIR Motion Detector IC

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Features

- Low power CMOS technology (ideal for battery operated PIR devices)
- CMOS high input impedance operational amplifiers
- Bi-directional level detector / Excellent noise immunity
- Built-in Power up disable & output pulse control logic
- Dual mode : retriggerable & non-retriggerable



Pin description

Pin Number	Symbol	Description
1	A	Retriggerable & non-retriggerable mode select (A=1 : re-triggerable)
2	VO	Detector output pin (active high)
3	RR1	Output pulse width control (Tx) * See definition below
4	RC1	Output pulse width control (Tx) *
5	RC2	Trigger inhibit control (Ti) *
6	RR2	Trigger inhibit control (Ti) *
7	Vss	Ground
8	VRF	RESET & voltage reference input (Normally high. Low=reset)
9	VC	Trigger disable input (VC >0.2Vdd=enable; Vc<0.2Vdd =disabled)
10	IB	Op-amp input bias current setting
11	Vdd	Supply voltage
12	2OUT	2 nd stage Op-amp output
13	2IN-	2 nd stage Op-amp inverting input
14	1IN+	1 st stage Op-amp non-inverting input
15	1IN-	1 st stage Op-amp inverting input
16	1OUT	1 st stage Op-amp output

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Tx = The time duration during which the output pin (Vo) remains high after triggering.

Ti = During this time period, triggering is inhibited. See timing charts for details.

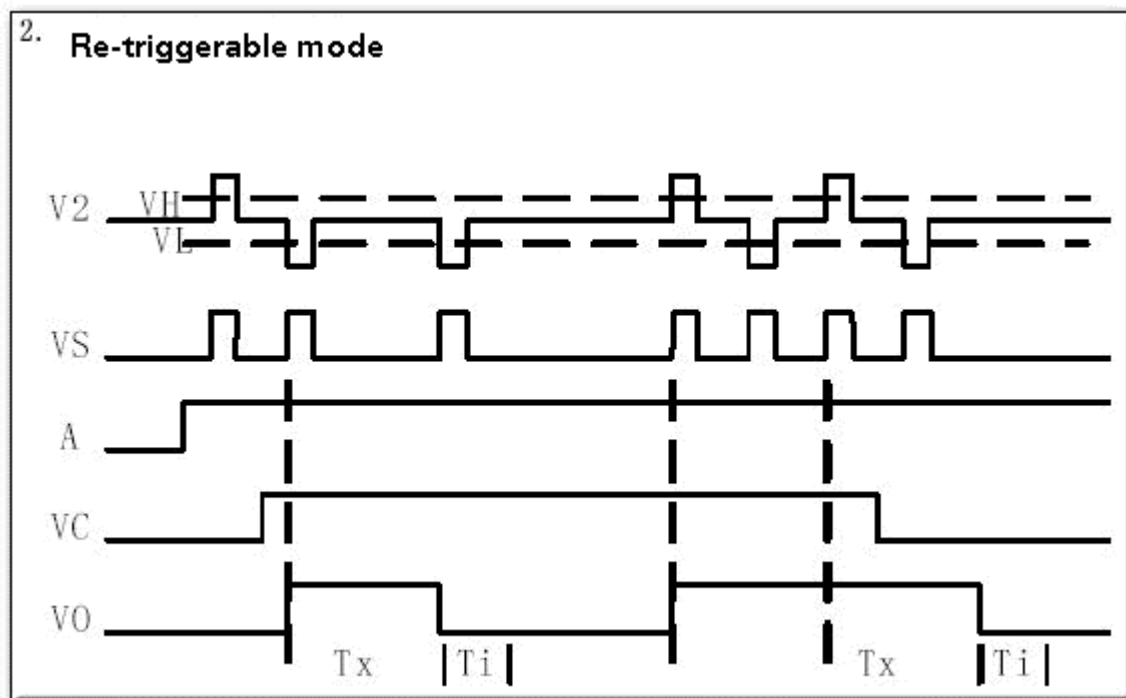
Tx ≈ 24576 xR10 x C6; **Ti** ≈ 24 x R9 x C7。 (ref to schematic)

Absolute max. ratings

Description	Condition	Range	Unit
Supply voltage	--	3 ~ 5	V
Input voltage	--	$V_{SS}-0.3 \sim V_{DD}+0.3$	V
Output current	$V_{DD}=5V$	10	mA
Operating temperature	--	-20 ~ +70	°C
Storage temperature	--	-40 ~ +125	°C

Retrigerrable waveform

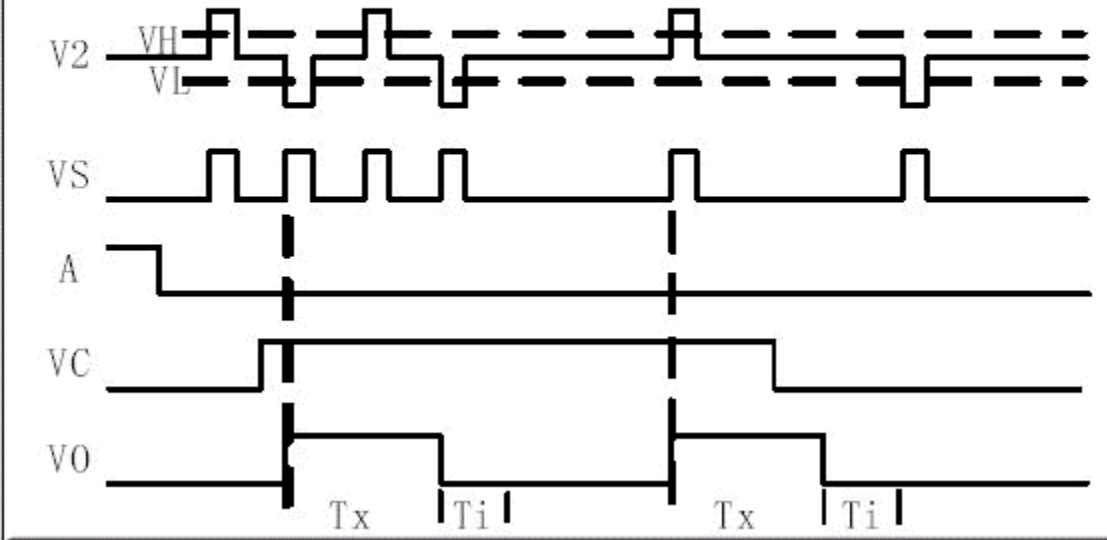
(NOTE : $V_H=0.7V_{DD}$, $V_L=0.3V_{DD}$)



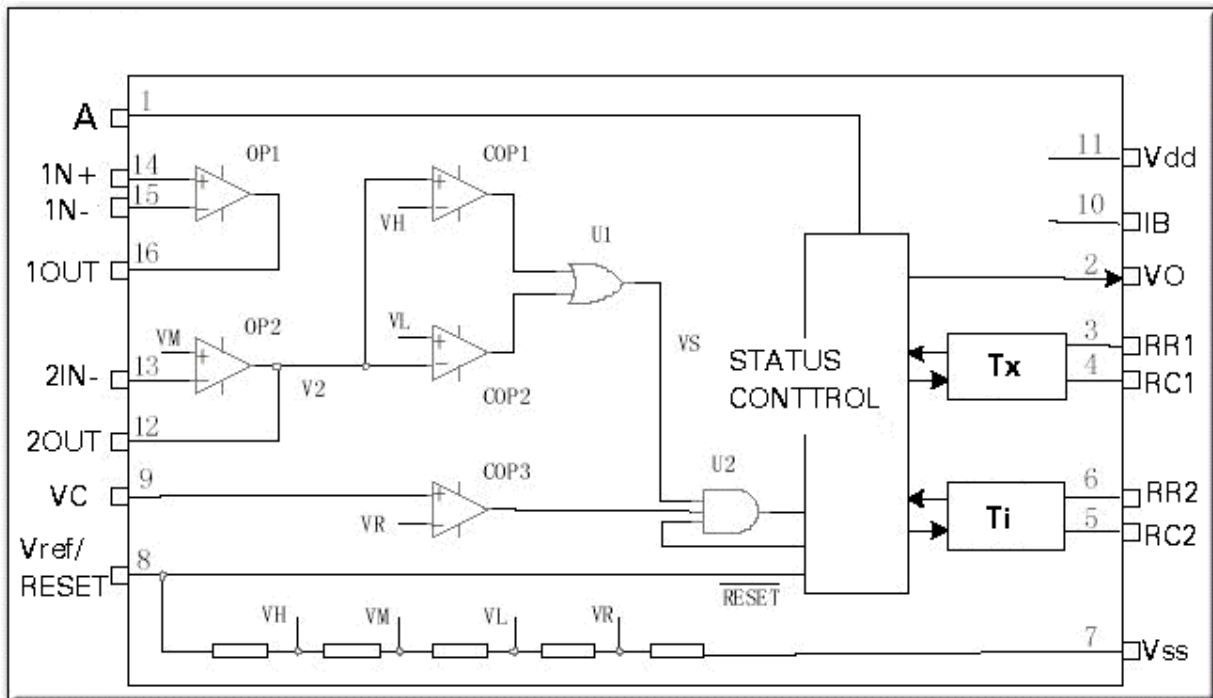
Non-retriggerable waveform

(NOTE : $V_H=0.7V_{dd}$, $V_L=0.3V_{dd}$)

1. NON-retriggerable mode



Internal Block Diagram



Tx - Output pulse width control

Ti - Trigger inhibit timing control

